CLAIMS

1. A system configured to provide fast acknowledgement and efficient servicing of an interrupt issued to a processor of an intermediate node, the system comprising:

an external device coupled to a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;

an interrupt multiplexing device accessible by the processor over a fast bus, the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device;

a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and

a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,

wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus.

2. The system of Claim 1 further comprising a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device.

3. The system of Claim 2 further comprising an interrupt handler invoked by the processor to service the issued interrupt.

4. The system of Claim 3 further comprising a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU.

5. The system of Claim 4 further comprising means for comparing a value of the last counter with a value of the current counter to determine whether there are more interrupts to service.

6. The system of Claim 5 wherein the means for comparing comprises the interrupt handler.

7. The system of Claim 1 wherein the external device is a direct memory access controller.

8. The system of Claim 1 wherein the low latency path is a printed circuit board trace.

9. The system of Claim 1 wherein the high latency path is a peripheral computer interconnect bus.

10. The system of Claim 1 wherein the interrupt multiplexing device is a field programmable gate array device.

11. A method for providing fast acknowledgement and efficient servicing of an interrupt issued to a processor of an intermediate node, the method comprising the steps of:

generating a pulsed interrupt signal at an external device coupled to a high latency path;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

invoking an interrupt handler to service the issued interrupt.

12. The method of Claim 11 further comprising the step of initializing a last counter.

13. The method of Claim 12 further comprising the steps of:
reading the status bit; and
if the status bit is clear, dismissing the handler.

14. The method of Claim 13 wherein the step of reading further comprises the step of clearing the status bit.

15. The method of Claim 13 further comprising the steps of:
if the status bit is set, reading a value of a current counter;
comparing the current counter value with a value of the last counter; and
if the last counter value is greater than or equal to the current counter value, returning to the step of reading the status bit.

16. The method of Claim 15 further comprising the steps of:
if the last counter value is not greater than or equal to the current counter value, checking a control block stored in a memory of the node, the control block shared between the processor and the external device; and
determining whether the processor owns the control block.

17. The method of Claim 16 further comprising the steps of:
if the processor owns the control block, processing the control block; and
incrementing the last counter.

18. The method of Claim 17 further comprising the steps of:
determining whether a preset limit for processing control blocks has been reached; and
if the preset limit is reached, dismissing the handler.

19. Apparatus for providing fast acknowledgement and efficient servicing of an interrupt issued to a processor of an intermediate node, the apparatus comprising:

means for generating a pulsed interrupt signal at an external device coupled to a high latency path;

means for transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

means for asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

means for issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

means for invoking an interrupt handler to service the issued interrupt.

20. A computer readable medium containing executable program instructions for providing fast acknowledgement and efficient servicing of an interrupt issued to a processor of an intermediate node, the executable program instructions comprising program instructions for:

generating a pulsed interrupt signal at an external device coupled to a high latency path;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

invoking an interrupt handler to service the issued interrupt.